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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,892	10/31/2003	Honkai Tam	SUNMP314	2989

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/698,892	TAM ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-14 and 16-20* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 1 is objected to because of the following informalities: the recitations " the rest voltage" and " second rest device" should be changed to " the reset voltage" and "second reset device". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, 6, 8-14 and 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (US Pat. 5,952,859).

Regarding claims 1 and 8, figures 1B and 1C show a method of resetting jam latch comprising:

combining a respective data signal (fb and reset) from each of a plurality of data lines connected to the input of circuit (36) to activate a first reset device (32);

activating a second reset device (38) with a control signal (in); and

applying a reset voltage (high level) to a storage cell (I1, I2).

When signal (pc-1) is low and signal (in) is low the first reset device (32) is turned on and the second reset device (38) is turned off. Thus, the supply voltage or reset voltage is applied across the first and second reset devices.

Regarding claim 2, combining the respective data in signal lines from each of the plurality of data lines to activate the first reset device includes:

coupling the respective data in signal from each of the plurality of data in signal lines to an activation device (36); and

outputting an activation signal (44) from the activation device (36) to the first reset device (32), when a level of the respective data in signal from each of the plurality of data lines is substantially equal (both data signals have high level to have a low level output 44 for activating the activating device 32).

Regarding claim 3, the control signal (in) is considered to be a clock signal.

Regarding claims 5 and 6, when the first reset device (32) is activated (ON), transistor (38) is turned off and the voltage source (GND) is disconnected from the storage cell (I1, I2).

Claims 9-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamamoto et al. (US Pub. 2002/0012280).

Regarding claims 9, figure 5 of Yamamoto shows a jam latch reset circuit comprising:

an activation device (AN0) having respective inputs coupled to each one of a plurality of data lines (rd, disa);

a first reset device (TR0) having a first control input (gate) coupled to an output of the activation device (AN0), the first reset device having a reset voltage (Vpre = 1.5V, [0141]) delivered by transistor (PRO) coupled to an input of the first reset device;

a second reset device (SE0) having a second control input (gate) coupled to a control signal (Y0), the second reset device being coupled in series with the first reset device; and

a storage cell (LA1) coupled to an output of the second reset device, the storage cell having an input and an output, the second reset device (SE0) having an output coupled to the storage cell output, and the storage cell input coupled to an input transistor (N10).

Regarding claims 10-13, the storage cell (LA1) is coupled to the second reset device (SE0). The control signal (Y0) is considered to be a timing signal and the activation device (AN0) is a logic device, an AND gate. The two signal lines are (rd) and (disa).

Regarding claims 14 and 16, the voltage source controller is transistor (N10).

Regarding claims 17 and 18, the signal lines are (rd) and (disa) and the storage includes a cross coupled inverter pair.

Regarding claims 19 and 20, figure 5 of Yamamoto shows a method of capturing data in a jam latch circuit comprising:

receiving a respective data in signal (rd, disa) on at least one of a plurality of data in signal lines;

charging a storage cell (LA1) on storage cell input with voltage (Vpre=1.5V).

outputting a data signal from a storage cell output;

combining (via element AN0) the respective data in signal from each of the plurality of data in signal lines and the data signal from the storage cell output;

outputting a jam latch output data signal; and

resetting a jam latch circuit including:

combining the respective data in signal from each of the plurality of data in signal lines to activate a first reset device;

activating a second reset device (SE0) with a control signal (YO); and

applying a reset voltage to the storage cell.

The input data (rd, disa0 are coupled to the activation device (AN0). The logic levels of the plurality of data in signals are substantially equal (inputs to AND gate).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US Pat. 5,952,859).

Regarding claim 4, figure 1B of Kim includes all the limitations of claim 4 except for the limitation that the control signal is inverted. However, it is old and well known in the art that a signal is inverted before inputting to an input of a circuit for matching with the required polarity of the input of that circuit. Therefore, it would have been obvious to those skilled in the art to invert the control signal (in) of transistor (38) is changed to the opposite type of transistor.

Allowable Subject Matter

Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 15 is objected to because the prior art of record fails to teach or fairly suggest a jam latch comprising a voltage source controller including an input coupled to the output of the activation circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.

Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
06-29-05

TUAN T. LAM
PRIMARY EXAMINER